REMARKS

Applicant concurrently files herewith a petition and fee for a two-month extension of time.

Claims 1-2, 4-13, 22-33, and 35-38 are presently pending in this application. Claims 1, 4-6, 10-13, 22, 26, and 30-32 have been amended to more particularly define the invention. Claims 3, 14, and 34 have been canceled in the interest of expediting prosecution. Non-elected claims 15-21 were previously canceled. Claims 35-38 have been added to assure Applicants the degree of protection to which their invention entitles them.

THE OFFICE ACTION

The Response to Second Office Action and Election of Species Requirement and Amendment filed March 22, 2004 traversed the requirement for election of species, added claims 30-34 which that Response stated were generic, amended other claims to conform with the newly added claims, elected the first species of Figures 1-9 with traverse, and stated that at least claims 1-4, 6-7, and 9-14 read on the elected species. The generic claims also read on the elected species. The Office Action of May 17, 2004 states that the traversal is "not persuasive because claims 31-33 contains [sic] species ... these species are mutually exclusive." *Assuming* that claims 31-33 are directed to species which are mutually exclusive, still claim 30 is generic. Thus, the traversal was not incorrect. If claim 30, or another generic claim is allowable, then Applicants are entitled to examination of their species claims.

With respect to the prior art rejections, claims 1-4, 6-9, 13-14, 30 and 34 were rejected under 35 U.S.C. §102(e) as being anticipated by Komada, U.S. Patent Publication No. 2002/0125577 A1, and claims 10-12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Komada in view of Ibnabdeljalil et al., U.S. Patent Publication No. 2002/0024115 A1. These rejections are respectfully traversed.

THE CLAIMED INVENTION

The claimed invention is directed to a semiconductor device which in an exemplary embodiment includes a semiconductor chip comprising a plurality of wiring insulating films 11, 13, 15, 16 stacked on top of each other in layers on a semiconductor substrate 1. A circuit formation portion 18 is provided within the semiconductor chip. One or more wiring trenches 35, 42, 49, 56 are formed in each of the wiring insulating films, along a periphery of the semiconductor chip, in such a manner as to surround a specified region on the semiconductor substrate. In each of the wiring trenches, a conductive layer 37, 44, 51, 58 is buried via a first conductive layer diffusion preventing film 36, 43, 50, 57. At least one conductive layer is connected to a diffusion region 19 formed in the semiconductor substrate.

Each wiring insulating film includes a low-dielectric constant film. At least one of the wiring insulation films comprises a low-dielectric constant film comprising methyl-silsesquioxane or hydrogen-silsesquioxane, or a low-dielectric constant film having a dielectric constant lower than or equal to that of methyl-silsesquioxane or of hydrogen-silsesquioxane.

Each wiring insulating film further includes a second conductive layer diffusion preventing film 32, 39, 46, 53, for example a silicon nitride film, in contact with a corresponding one of the first conductive layer diffusion preventing films.

THE PRIOR ART REFERENCES

The Komada Reference

Komada discloses a semiconductor integrated circuit device with a "moisture-proof" ring area and a "device" area. The semiconductor integrated circuit device has a plurality of

interlevel insulating films 47, 53, 58, 66, 68, 74, 76. The "moisture-proof" ring area includes a moisture-proof ring made up of conductive regions 51r, 55r, 63r, 71r, 79r that pass through the insulating films to contact an insulator ring 41r in a silicon substrate 40. In paragraph 0073, Komada states that the first interlevel insulating film 47 is made of an insulator having a low dielectric constant such as fluorine-containing silicon glass (fluorine-containing silicon oxide).

The "device" area includes conductive regions 51c, 55c, 63c, 71c, 79c that pass through the insulating films to contact an n-type source/drain region 42n.

It is to be noted that it is the conductive regions of the "device" area that contact the n-type region 42n, while the conductive regions of the "moisture-proof" ring area contact an insulator ring 41r.

The insulating films are separated by etching stopper layers which contact barrier layers around the respective conductive layers.

The Ibnabdeljalil et al. Reference

Ibnabdeljalil discloses an insulator device having sacrificial structures for arresting insulator cracks. A plurality of individual seal structures 20c-24c are provided within a plurality of interlayer insulation films 31, 34, 37, 40. Each seal structure consists of a multitude of patterned metal layers 33, 36, 39, 42 positioned on top of each other and mutually connected by metal-filled via grooves 32, 35, 38, 41. A lowermost via groove 27 contacts a heavily-doped region 28 or moat 30, within a semiconductor substrate 29a, 29b.

ARGUMENT

In the claimed invention, a conductive layer diffusion preventing film 32, 39, 46, 53

is formed between adjacent wiring insulating films. This feature is included in each claim.

In Komada's device, the insulating films are separated only by etching stopper layers.

Likewise, Ibnabdeljalil's device does not have a conductive layer diffusion preventing film formed between adjacent wiring insulating films.

Further, while Komada states that his first interlevel insulating film 47 is made of an insulator having a low dielectric constant such as fluorine-containing silicon glass, there is no showing or suggestion in either Komada or Ibnabdeljalil of at least one of the wiring insulation films comprising a low-dielectric constant film comprising methyl-silsesquioxane or hydrogen-silsesquioxane, or a low-dielectric constant film having a dielectric constant lower than or equal to that of methyl-silsesquioxane or of hydrogen-silsesquioxane, as in the claimed invention.

There is thus no suggestion in either Komada or Ibnabdeljalil, or the combination of the two, that would lead a person of ordinary skill in the art to the claimed invention. It is accordingly submitted that the claims are allowable.

FORMAL MATTERS

Minor corrections have been made to the specification and the drawings to assure consistency.

CONCLUSION

In view of the foregoing, Applicant submits that claims 1-2, 4-13, 22-33, and 35-38, all the claims presently pending in the application, are patentably distinct over the prior art of record and that the application is in condition for allowance. Such action would be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below to discuss any other changes deemed necessary for allowance in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Attorney's Deposit Account No. 50-0481 and please credit any excess fees to such deposit account.

Respectfully Submitted,

Date: December 28, 2007

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AMENDMENTS TO THE DRAWINGS

Figure 17 is amended by changing the reference designation "71; seal ring" to "70" to agree with the specification at page 41, line 12.

Figure 18 is amended by redirecting the lead line from reference numeral 70A to point to the exposed face of assembly pad 70, to agree with the specification at page 45, line 13.

Figure 19 is amended by changing the reference designation "79; bottomed portion of conductive layer" to "79; bottom portion of conductive layer" to agree with the specification at, *inter alia*, page 46, lines 16-17.

Figure 20 is amended by redirecting the lead line from reference numeral 70A to point to the exposed face of assembly pad 70, to agree with the specification at page 48, lines 22-23 and page 43, line 3.